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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/752,396	12/28/2000	Cheon-Soo Kim	51876P231	9505

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No. 09/752,396	Applicant(s) KIM ET AL.	
	Examiner ori nadav	Art Unit 2811	

-- The MAILING DATE f this communication appears n the cover sheet with the correspondence address --

Peri d f r R ply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) *5-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim R jections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. (6,242,787) in view of Applicant Admitted Prior Art (AAPA).

Regarding claim 1, Nakayama et al. teach in figure 8 and related text (column 12, line 27 to column 13, line 21) a HF power device in an HF transistor comprising a first semiconductor layer 121b as a first conductive type, a second semiconductor layer 121a formed on the first semiconductor layer, a field area having a trench structure 123 (column 8, line 33) formed in the second semiconductor layer; gate electrode 107 formed on the second semiconductor layer, a channel layer 102 as a second conductive type formed from isolation area 129 to a width containing both sides of the gate electrode in the second semiconductor layer, and formed on the surface of the semiconductor layer; a source area 104 as the second conductive type formed within the channel layer between one side of the gate electrode and the field area; a drain area 105 as the second conductive type formed in the second semiconductor layer with a given interval from the other side of the gate electrode; a sinker 112 (P+ and P

regions) as the first conductive type provided as a column shape of a trench structure for dividing into two source areas by a piercing through the source area and the second semiconductor layer, and connected to the first semiconductor layer (via a PN diode); first metal electrode 110 connected with the source area and electrically connected to the second semiconductor layer through the sinker (and through P well 116); and second metal layer electrode 111 coupled with the drain area.

Note that since Nakayama et al.'s device is formed in the second semiconductor layer 121a, then channel layer 102 is also formed in the second semiconductor layer, and sinker 112 is piercing through the second semiconductor layer (since the second semiconductor layer 121a includes P well 116 therein, and sinker 112 is piercing through P well 116).

Note that the claimed limitation of a sinker provided as a column shape of a trench structure does not require the sinker to have a trench structure, but only a column shape of a trench structure. Nakayama et al.'s sinker has a column shape, which is the shape of a trench structure. Therefore, Nakayama et al. teach a sinker having a column shape of a trench structure, as claimed.

Nakayama et al. do not teach in the embodiment of figure 8 a channel layer formed from the field area and an LDD area as the second conductive type formed on the surface of the semiconductor layer between the drain area and the gate electrode;

Nakayama et al. teach in the embodiment of figure 4 a channel layer N formed from the field area 23 (the channel layer N of LDMOS is formed from the left field area 23).

AAPA teaches in figure 1 and related text (pages 1-3) an LDD area 18 as the second conductive type formed on the surface of the semiconductor layer between the drain area 19 and the gate electrode 15.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the channel layer from the field area and to use an LDD area as the second conductive type formed on the surface of the semiconductor layer between the drain area and the gate electrode in Nakayama et al.'s device in order to simplify the processing steps of making the device and in order to improve short channel effects and the electrical characteristics of the device, respectively.

Regarding the process limitations of a channel layer laterally diffuses, as recited in claim 1, and a field area being any one among an oxide film grown in the trench, an oxide film gained by performing a covering on the trench and then by executing a burying there into through a use of a CMP, and a thermal oxide film gained by performing a thermal oxidation for the trench, as recited in claim 4, these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685;

In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

2. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. and AAPA, as applied to claim 1 above, and further in view of Tihanyi (6,326,656).

Regarding claims 2 and 3, Nakayama et al. and AAPA teach substantially the entire claimed structure, as applied to claim 1 above, except forming a sinker being as one or a plural number of trench structures doped with impurity of the first conductive type on the neighborhood thereof, wherein the trench structure having a burying of polysilicon film based on the first conductive type there into. Tihanyi teach in figure 1 and related text (column 3, lines 10-18) a sinker 8 being provided as one or a plural number of trench structures doped with impurity of the first conductive type on the neighborhood thereof, wherein the trench structure having a burying of polysilicon film based on the first conductive type there into.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the sinker as one or a plural number of trench structures doped with impurity of the first conductive type on the neighborhood thereof, wherein the trench structure having a burying of polysilicon film based on the first conductive type there into in Nakayama et al. and AAPA's device in order to simplify the processing steps and to improve the characteristics of the device by providing more accurate doping concentration and dimensions of the sinker.

Response to Arguments

3. Applicant argues that Nakayama et al. do not teach a sinker being formed with a trench structure.

The claimed limitation of a sinker provided as a column shape of a trench structure does not require the sinker to have a trench structure, but only a column shape of a trench structure. Nakayama et al.'s sinker has a column shape, which is the shape of a trench structure. Therefore, Nakayama et al. teach a sinker having a column shape of a trench structure, as claimed.

4. Applicant argues that AAPA does not disclose a sinker being formed with a trench structure.

AAPA is not cited to teach an artisan that a sinker being formed with a trench structure. AAPA is cited to teach an artisan that an LDD area 18 as the second conductive type formed on the surface of the semiconductor layer between the drain area 19 and the gate electrode 15.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
November 3, 2003

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800